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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Yoshimasa Ogawa

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EXAMINER

SELBY, GEVELL V

ART UNIT

PAPER NUMBER

2622

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/775,639

Applicant(s)

OGAWA, YOSHIMASA

Examiner

Gevell Selby

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 8-12, 18 and 20-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 18, 20, 21, 23, 24 and 26 is/are allowed.
- 6) ☒ Claim(s) 1-4, 8-12, 22 and 25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see the amendment, filed 6/13/06, with respect to the rejection(s) of claim(s) 1-4, and 8-12 under 35U.S.C. 102 and 103 rejections have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Morimoto.

2. Applicant's arguments filed 6/13/06 have been fully considered but they are not persuasive. The applicant submits the prior art does not disclose the following limitations of the claimed invention:

a plurality of k line buffers each line buffer holding up to m pixels of image data, and the number of the plurality line buffers arranged in the vertical direction is a value which is more than 1 and less than v, as stated in claims 22 and 25. The Examiner respectfully disagrees.

Examiner's Reply:

Re claims 22 and 25) The Morimoto reference discloses a plurality of k line buffers (see figure 3, element 102a-d), each line buffer holding up to m pixels of image data, and the number of the plurality line buffers arranged in the vertical direction is a value which is more than 1 and less than v (see figure 3 and column 7, lines 14-27: each imaging section 101a-d staged in the vertical direction has one register for multiple columns of the image sensor, making v greater the number of registers or line buffers).

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-4, 22, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Morimoto, US 5,969,759.**

In regard to claim 1, Morimoto, US 5,969,759, discloses a solid-state imaging element, comprising:

a plurality of light-receiving sensors (see figure 3, elements 101a-d) converting optical signals to electrical signals (see column 5, lines 9-19), the plurality of light-receiving sensors arranged in v x h (vertical x horizontal) matrix (see figure 3, elements 101-1); and

a memory (see figure 3, elements 102a-d) storing the electrical signals as optical image data, said memory being formed of a plurality of line buffers (see column 5, lines 16-21), and the number of the plurality of line buffers arranged in the vertical direction is a value which is more than 1 and less than v (see figure 3:

Art Unit: 2622

each imaging section 101a-d staged in the vertical direction has one register for multiple columns).

In regard to claim 2, Morimoto, US 5,969,759, discloses the solid-state imaging element of claim 1, further comprising:

a first switch circuit connecting one of the line buffers and said light-receiving sensors (see column 5, line 39 to column 6, line 34: transfer gates).

In regard to claim 3, Morimoto, US 5,969,759, discloses the solid-state imaging element of claim 2, wherein the data in the line buffers are output in parallel (see column 7, lines 19-26).

In regard to claim 4, Morimoto, US 5,969,759, discloses the solid-state imaging element of claim 1 comprising:

a switch circuit selecting one of the line buffers to output the electrical signal (see figure 3, elements 103a-d: output sections).

In regard to claims 22 and 25, Morimoto, 5,969,759 discloses a charge-coupled device (CCD) and the method of outputting image data from the CCD, comprising:

an array of photosensors (see figure 3) arranged in v vertical lines and horizontal lines corresponding to an $n \times v$ pixel array of image data (see column 5, lines 9-16), each horizontal line being divided into k line sections, each line section corresponding to m ($m < k$) pixels of image data the plurality of photosensors arranged in $v \times h$ (vertical \times horizontal) matrix (see column 5, lines 16-21); and

a plurality of k line buffers (see figure 3, element 102a-d), each line buffer holding up to m pixels of image data, and the number of the plurality line buffers arranged in the vertical direction is a value which is more than 1 and less than v (see figure 3: each imaging section 101a-d staged in the vertical direction has one register for multiple columns), wherein blocks of n.times.m pixels of image data are transferred from the array of photosensors to the line buffers, such that a first one of the buffers receives m pixels from a horizontal line and outputs the m pixels before receiving another m pixels from the next horizontal line and so forth until a first block of n.times.m pixels has been transferred and output, and repeating the transfer and output operations for each remaining line buffer and the remaining image data (see column 7, lines 8-27).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morimoto, US 5,969,759, in view of Juen, US 5818,524.**

In regard to claim 8, Morimoto, US 5,969,759, discloses an image processor, comprising:

a solid-state imaging element (see figure 3) comprising a plurality of light receiving sensors to convert optical signals to electrical signals (see column 5, lines 9-22), the plurality of light-receiving sensors arranged in $v \times h$ (vertical \times horizontal) matrix (see figure 3, elements 101-1); and

an electrical signal holder (see figure 3, elements 102a-d) within said solid-state imaging element comprising line buffers (see column 5, lines 16-22), wherein the number of the plurality of line buffers arranged in the vertical direction a value which is more than 1 and less than v (see figure 3: each imaging section 101a-d staged in the vertical direction has one register for multiple columns).

The Morimoto reference does not disclose an encoder encoding the electrical signals in units of $n \times m$ pixels.

Juen, US 5,818,524, discloses a digital still image camera with an irreversible encoder that codes image data before saving onto a recording medium (see figure 2, element 28 and column 4, lines 5-20).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Morimoto, US 5,969,759, in view of Juen, US 5,818,524, to have an encoder encoding the electrical signals in units of $n \times m$ pixels in order to compress image data output from the image sensor so the more data may be stored on a recording medium.

Art Unit: 2622

In regard to claim 9, Morimoto, US 5,969,759, in view of Juen, US 5818,524, discloses the image processor of claim 8. The Morimoto reference discloses further comprising:

a first switch circuit connecting one of the line buffers and the light receiving sensors (see column 5, line 39 to column 6, line 34: transfer gates).

In regard to claim 10, Morimoto, US 5,969,759, in view of Juen, US 5818,524, discloses the image processor of claim 9. The Morimoto reference discloses wherein data in the line buffers are output in parallel (see column 7, lines 19-26).

In regard to claim 11, Morimoto, US 5,969,759, in view of Juen, US 5818,524, discloses the image processor of claim 8. The Morimoto reference discloses further comprising:

a switch circuit selecting one of the line buffers to output the electrical signal (see figure 3, elements 103a-d: output sections).

In regard to claim 12, Morimoto, US 5,969,759, in view of Juen, US 5818,524, discloses the image processor of claim 8, wherein said encoder is a JPEG encoder (see Juen: see column 4, lines 13-15).

Allowable Subject Matter

8. Claims 18, 20-21, 23, 24, and 26 are allowed.
9. The following is a statement of reasons for the indication of allowable subject matter: claims 18, 20-21, 23, 24, and 26 are allowable for the reason stated in the previous office action.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gevell Selby whose telephone number is 571-272-7369. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on 571-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

gvs



VIVEK SRIVASTAVA
PRIMARY EXAMINER